

File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)

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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200409

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File 348:EUROPEAN PATENTS 1978-2004/Jan W05

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File 349:PCT FULLTEXT 1979-2002/UB=20040205,UT=20040129

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Set	Items	Description
S1	42	AU=JOURDAN S?
S2	19	S1 AND CACH???
S3	9	S2 AND PREDICT?
S4	2	S3 AND (SIMULTANEOUS? OR CONCURREN? OR COINCIDENT? OR PARALLEL)

4/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015599597 **Image available**
WPI Acc No: 2003-661752/200362
XRPX Acc No: N03-528028

Processor instructions fetching method, involves receiving instruction request and searching cache system for instruction at initial level and next level parallelly based on initial level parameter

Patent Assignee: JOURDAN S (JOUR-I)

Inventor: JOURDAN S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030126366	A1	20030703	US 200233112	A	20020102	200362 B

Priority Applications (No Type Date): US 200233112 A 20020102

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030126366	A1		10	G06F-013/00	

Abstract (Basic): US 20030126366 A1

NOVELTY - The method involves receiving a request for an instruction and searching a **cache** system at an initial level for the instruction. A parameter corresponding to the initial level is determined and is compared with a predetermined threshold value and when exceeds the threshold value the **cache** system is searched at a next level for the instruction in **parallel** with the initial level.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a computer readable storage medium storing a set of instructions capable of being executed by processor

(b) a processor instruction management system.

USE - Used for fetching processor instructions.

ADVANTAGE - The time required to search the initial level is significantly shorter than the time required for searching the next level, thereby increasing the processor speed.

DESCRIPTION OF DRAWING(S) - The drawing shows a flowchart of a method of **predicting** a trace **cache** miss.

pp; 10 DwgNo 3/7

Title Terms: PROCESSOR; INSTRUCTION; FETCH; METHOD; RECEIVE; INSTRUCTION; REQUEST; SEARCH; **CACHE** ; SYSTEM; INSTRUCTION; INITIAL; LEVEL; LEVEL; BASED; INITIAL; LEVEL; PARAMETER

Derwent Class: T01

International Patent Class (Main): G06F-013/00

File Segment: EPI

PE/5/2

4/5/2 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01019923

METHOD AND APPARATUS FOR IDENTIFYING CANDIDATE VIRTUAL ADDRESSES IN A CONTENT-AWARE PREFETCHER

PROCEDE ET DISPOSITIF POUR IDENTIFIER DES ADRESSES VIRTUELLES DE CANDIDATS DANS UN SYSTEME DE LECTURE ANTICIPEE CONSCIENT DU CONTENU

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Application: WO 2002US38706 20021202 (PCT/WO US0238706)
Priority Application: US 2001549 20011130

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CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SI SK
TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: G06F-012/08

Publication Language: English

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Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 8267

English Abstract

A method and apparatus for identifying virtual addresses in a **cache** line. To differentiate candidate virtual addresses from data values and random bit patterns, the upper bits of an address-sized word in the **cache** line are compared with the upper bits of the **cache** line's effective address. If the upper bits of the address-sized word match the upper bits of the effective address, the address-sized word is identified as a candidate virtual address.